

### REMARKS

In response to the Office Action mailed July 29, 2003, reconsideration and further examination are hereby requested.

In the outstanding Office Action, the Examiner objected to the drawings for not showing the proposed changes in red. Thus, enclosed herewith are the proposed drawing amendments with all changes marked in red. Further, new formal drawings incorporating the changes are also filed herewith.

In item 2 on page 2 of the Office Action, the Examiner required a substitute specification. Thus, the present amendment seeks to amend the specification by replacing the specification with the enclosed substitute specification. Since this is a reissue application, the substitute specification includes bracketing and underlining to show the changes relative to the patent specification.

As indicated in item 3 of the Office Action, a Supplemental Reissue Declaration must be received before the reissue application can be allowed. Accordingly, a Supplemental Reissue Declaration is filed herewith including a statement that all errors being corrected in the reissue application, including any errors not covered by a prior declaration in this reissue application, up to the time of filing of the present declaration arose without any deceptive intention.

In view of the above, it is submitted that the present application is clearly in condition for allowance. The Examiner is invited to contact the undersigned attorney by telephone if necessary to expedite allowance of the application.

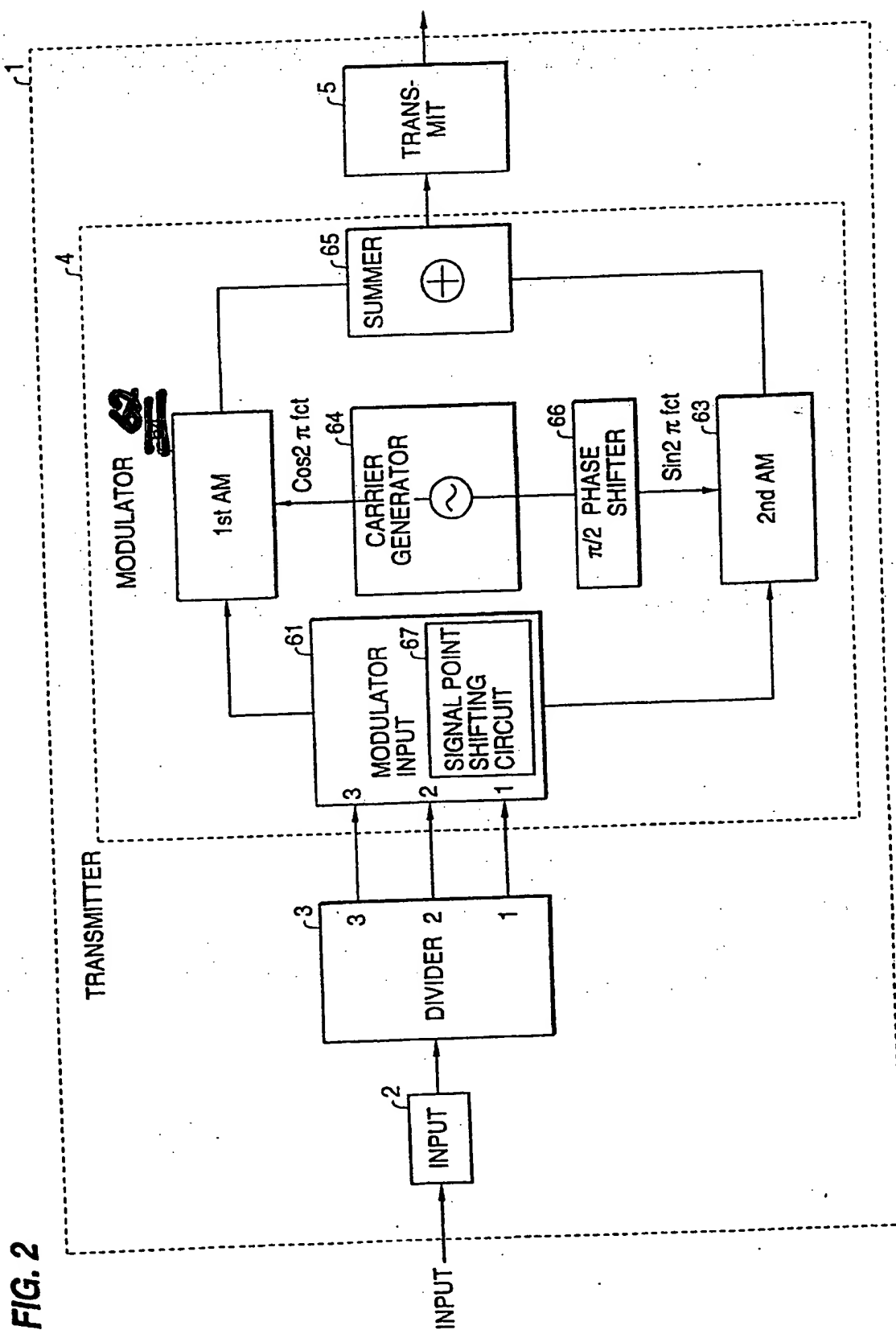
Respectfully submitted,

Mitsuaki OSHIMA et al.

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September 29, 2003



**FIG. 10**

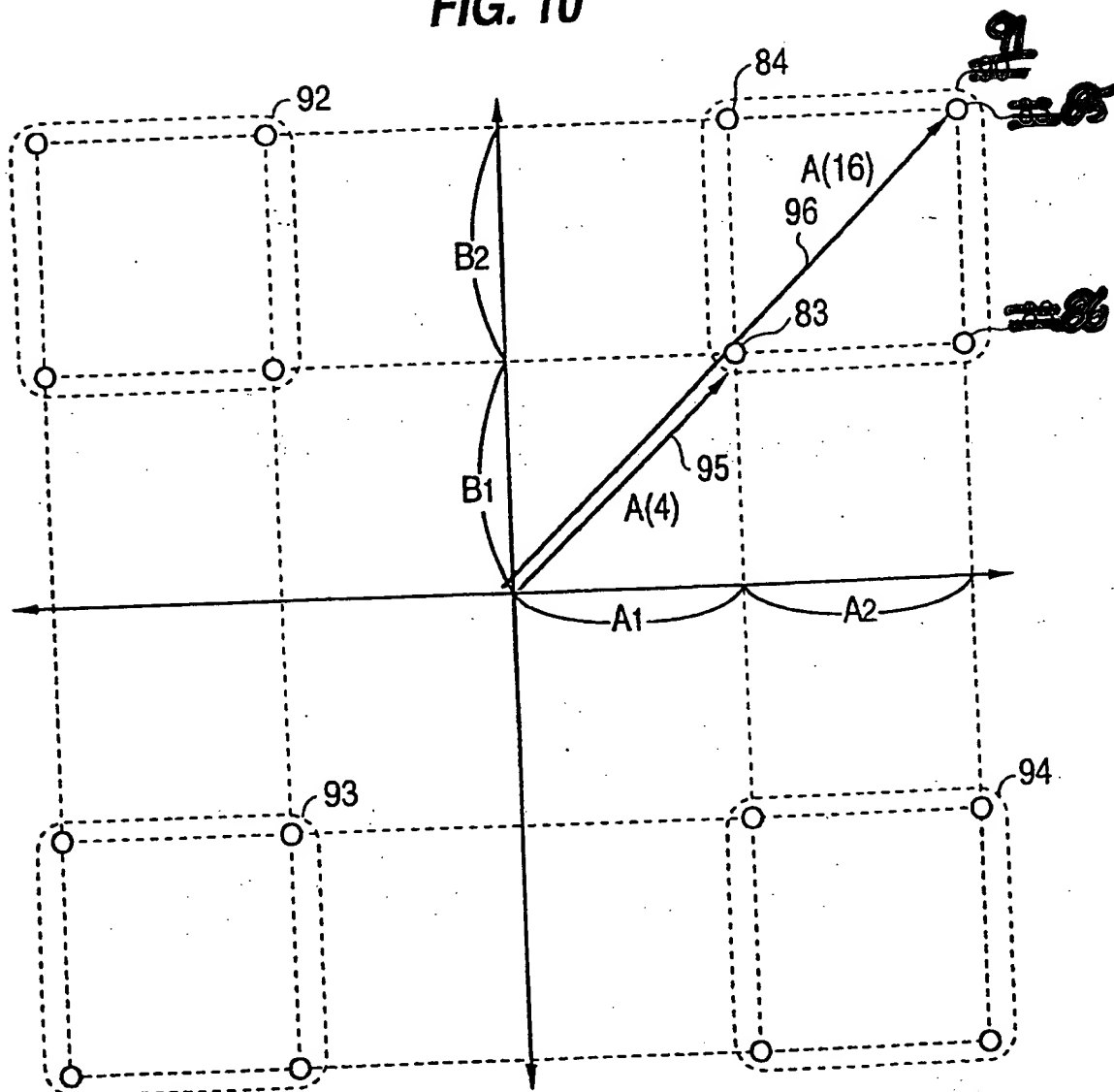
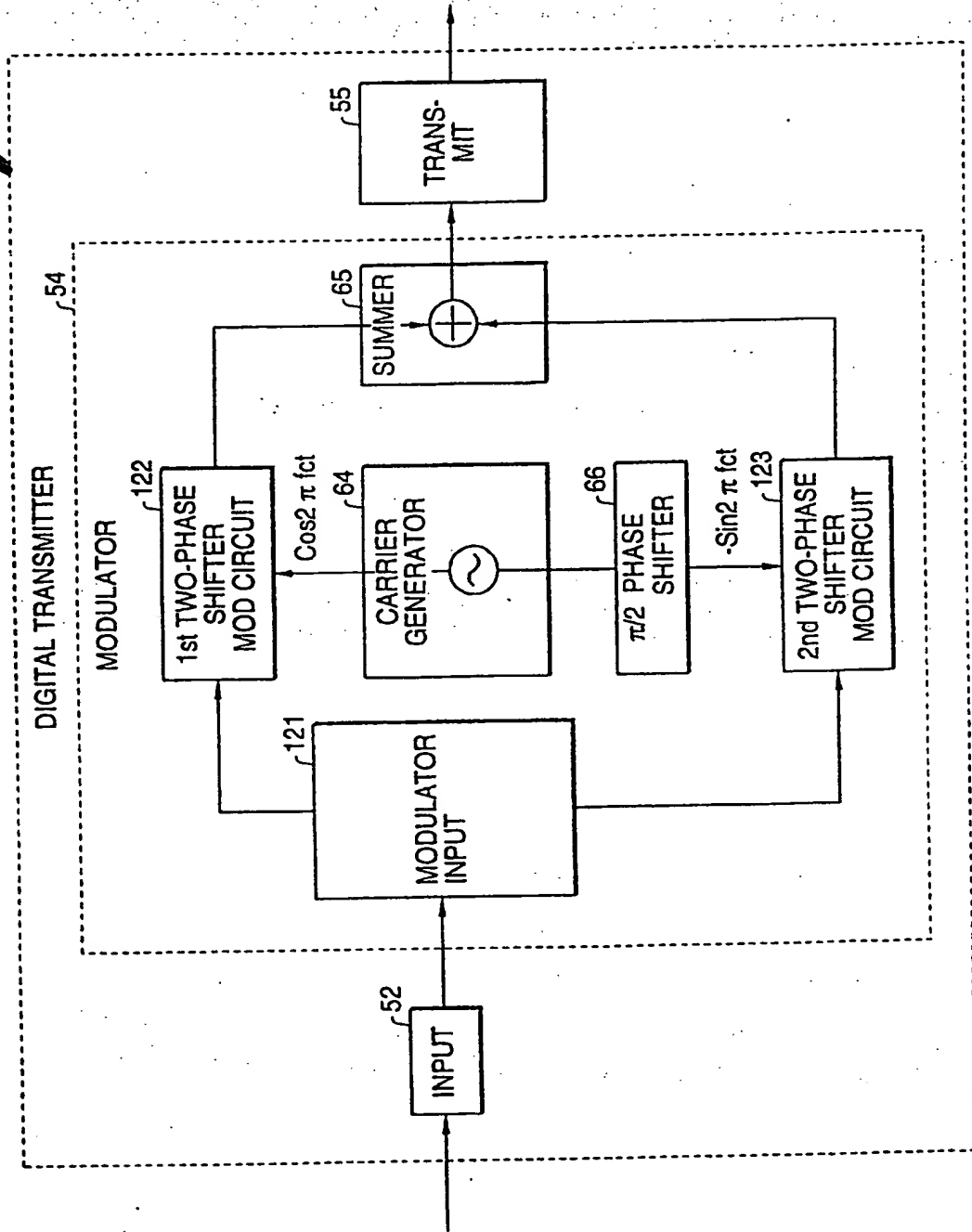


FIG. 17



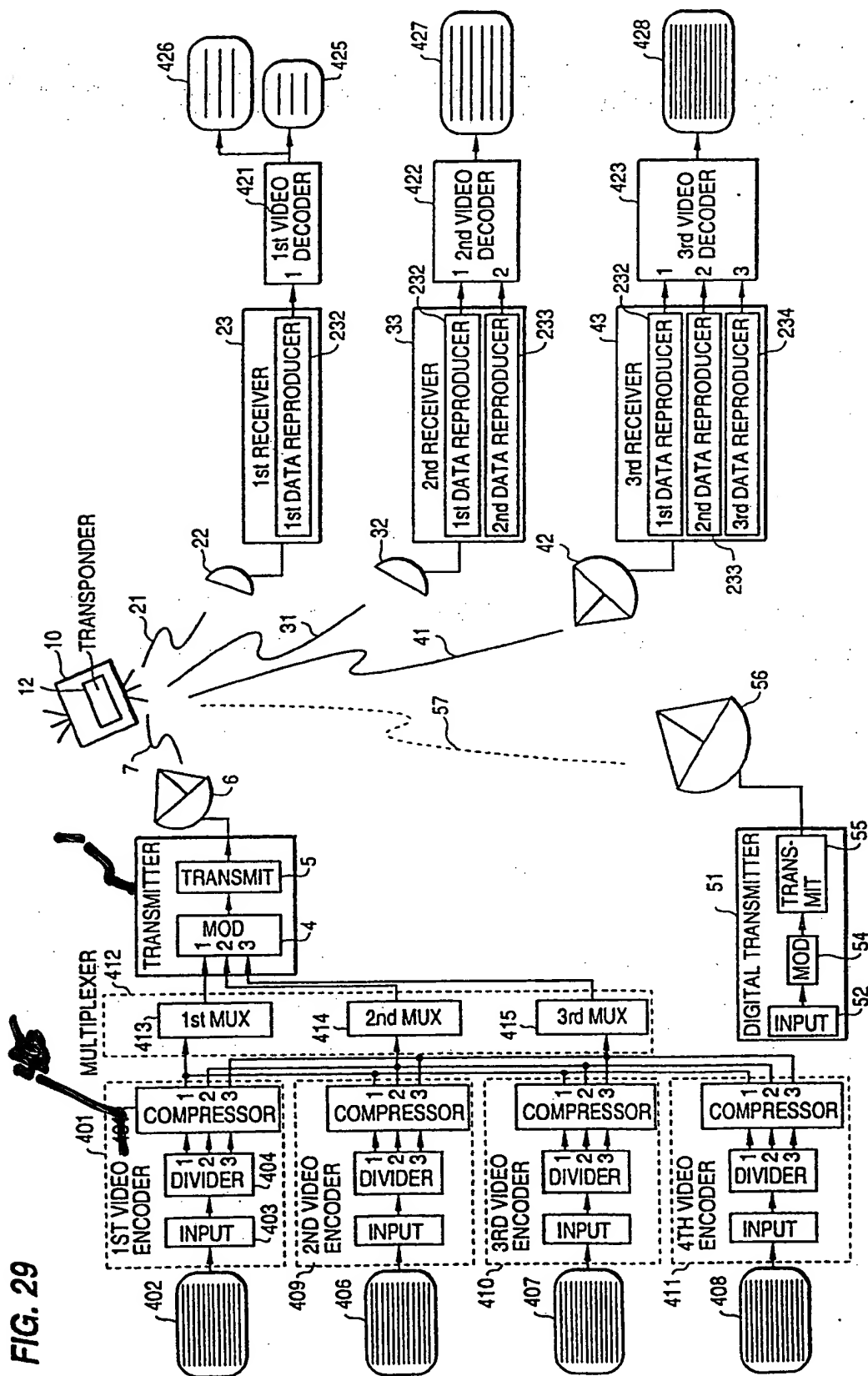


FIG. 48

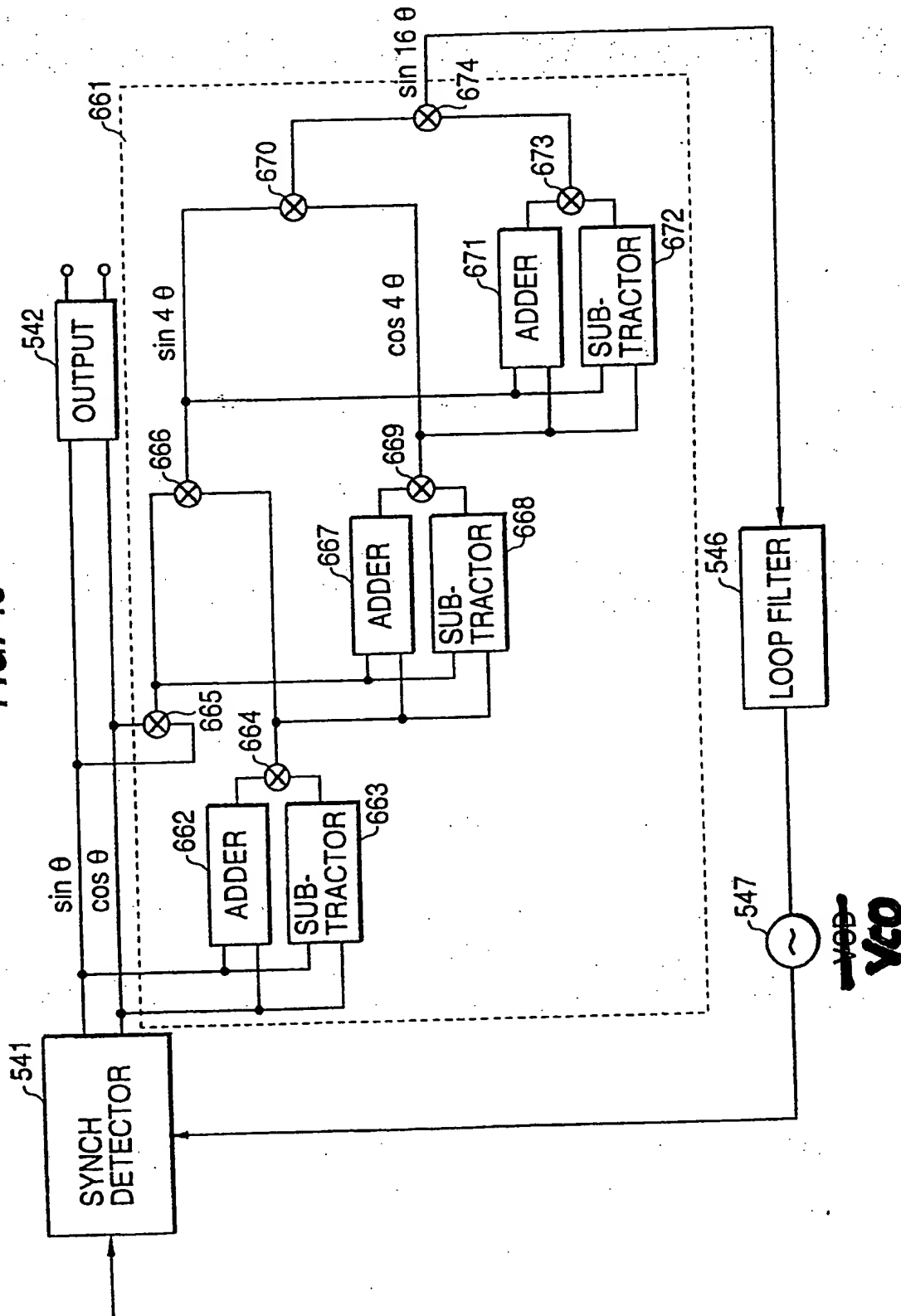
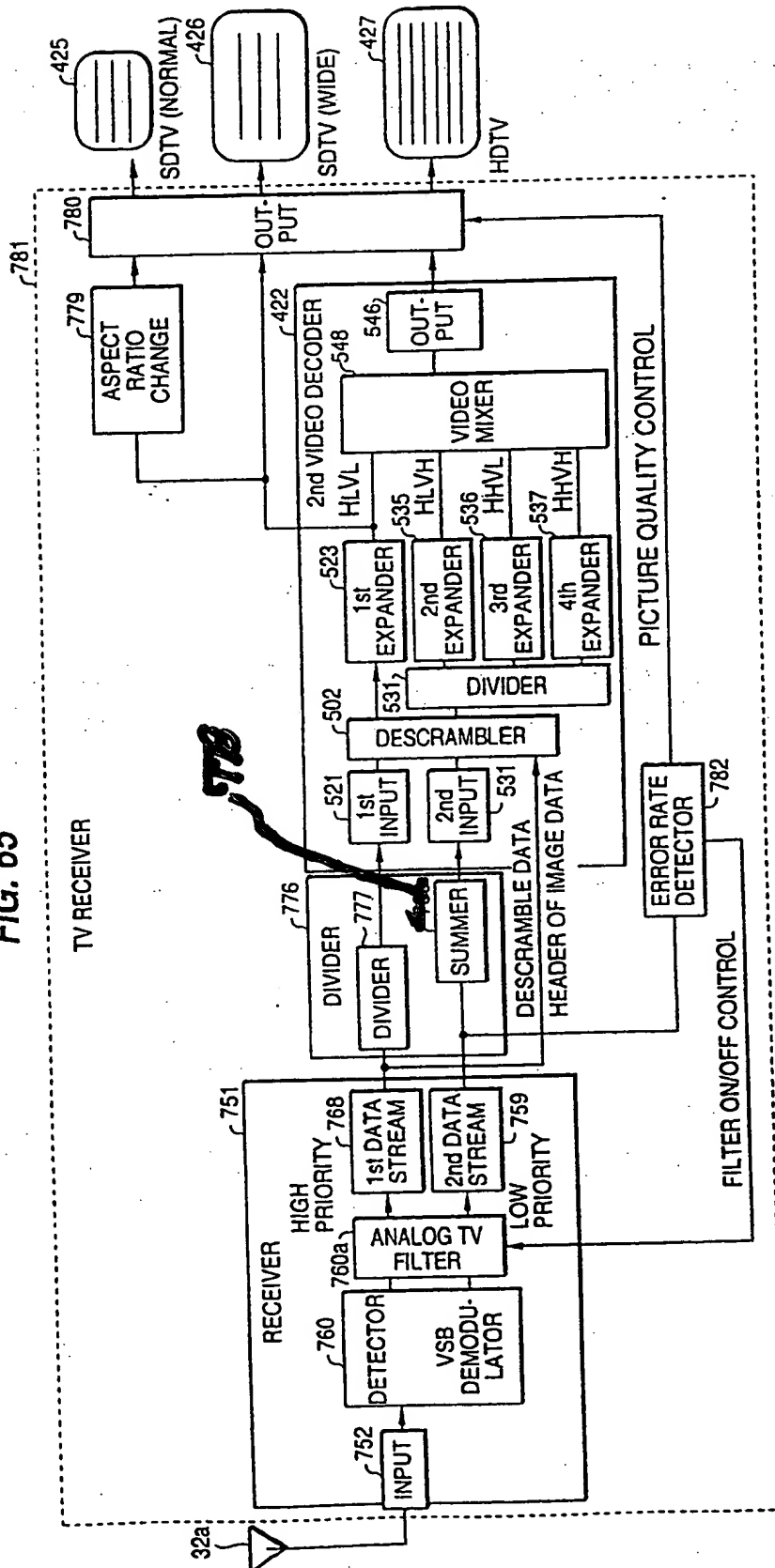


FIG. 65



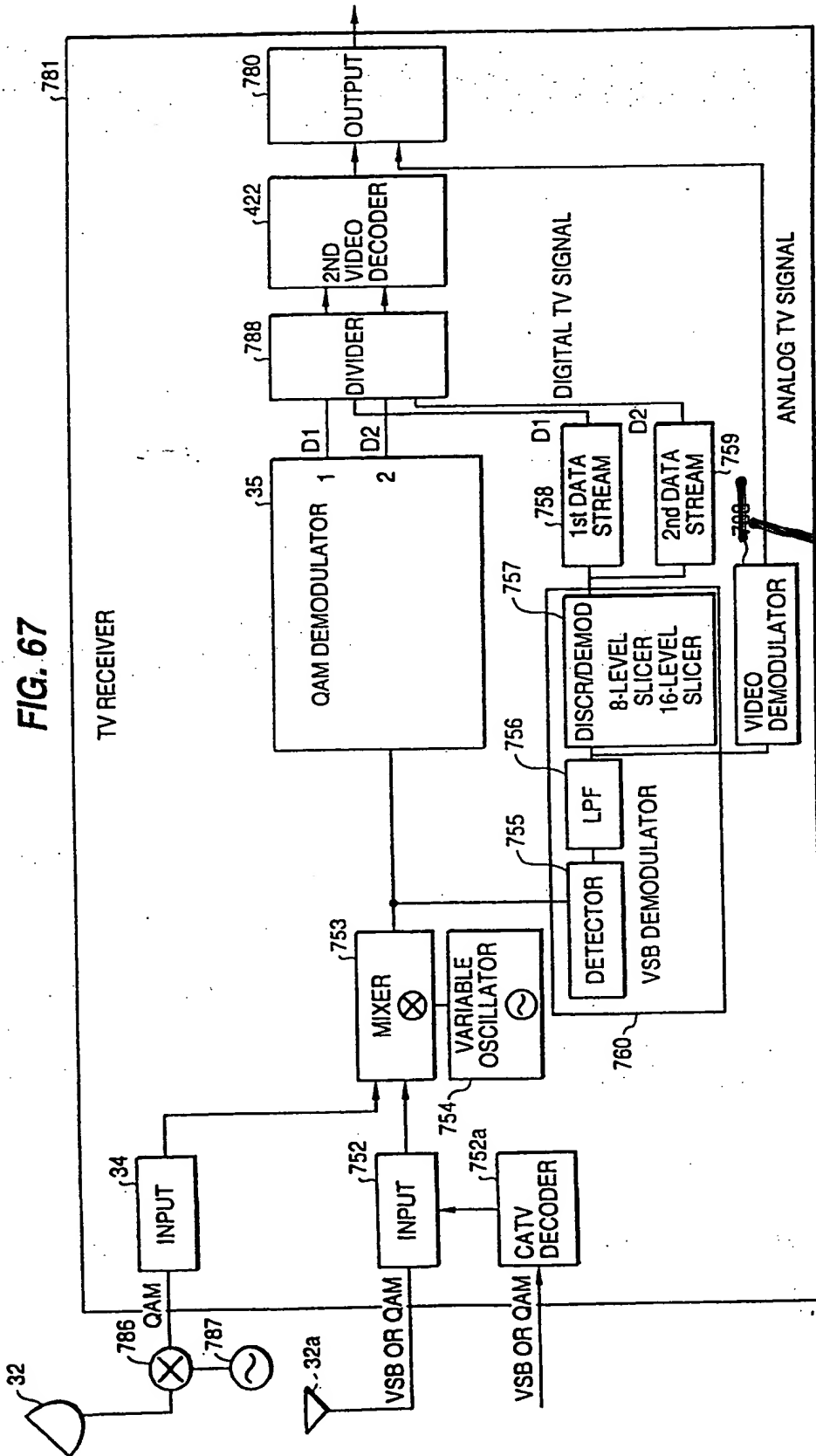


FIG. 93

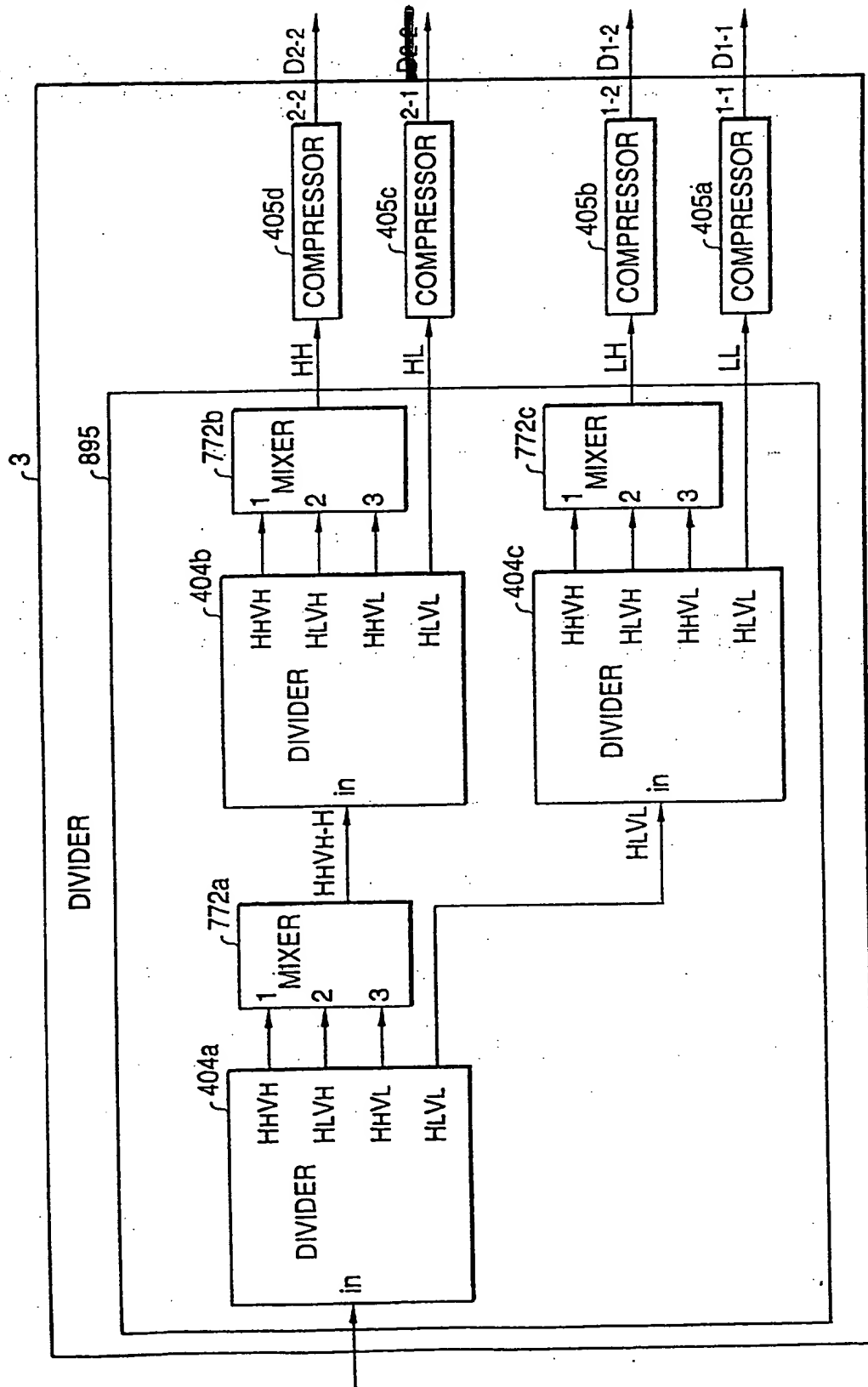
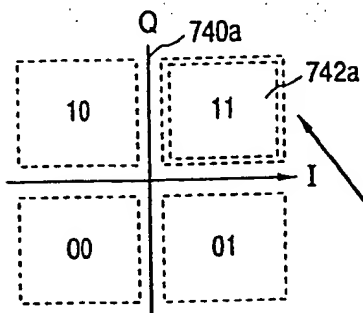
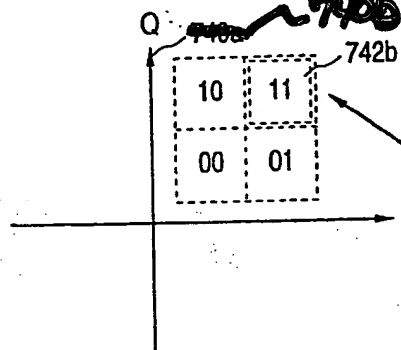


FIG. 112

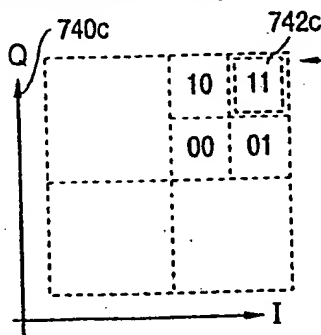
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



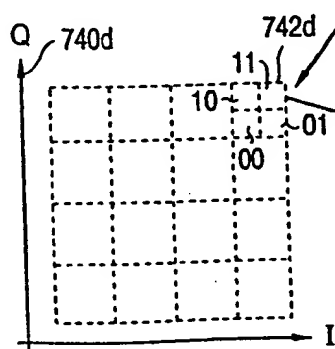
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)



SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)

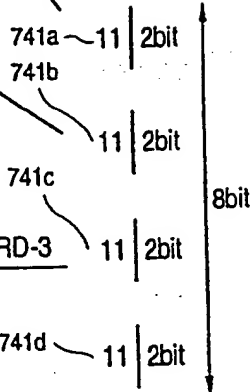


CODE WORD-1

CODE WORD-2

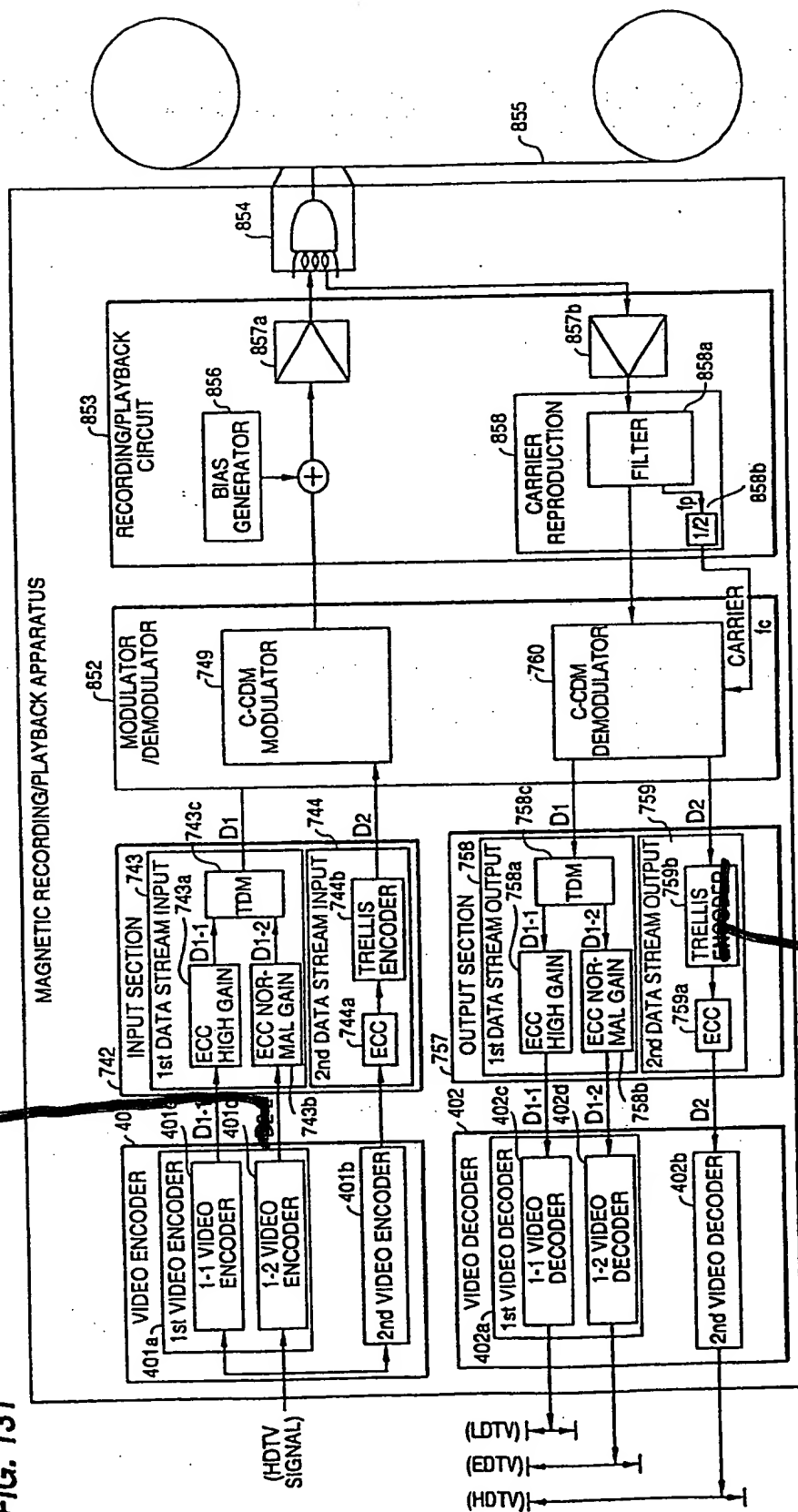
CODE WORD-3

CODE WORD-4





SIGNAL POINT  
CODE WORD  
11 11 11 11

**FIG. 131**



**Order**

(LDTV) |  |

(EDTV) |  |


(HDTV) |  |

FIG. 138

The diagram illustrates a transmitter and receiver system for OFDM-C-CDM modulation.

**TRANSMITTER:**

- VIDEO ENCODER (401a):** Processes the **(HDTV SIGNAL)** into a **1st VIDEO ENCODER** and a **2nd VIDEO ENCODER**.
- 1st DATA STREAM INPUT (743):** Receives output from the 1st video encoder, passes it through **ECC** and **HIGH GAIN** blocks, and then through a **D1-1** block.
- 2nd DATA STREAM INPUT (744):** Receives output from the 2nd video encoder, passes it through **ECC** and **MAL GAIN** blocks, and then through a **D1-2** block.
- TRELLIS ENCODER (744a):** Receives inputs from the **D1-1** and **D1-2** blocks.
- SERIAL TO PARALLEL (791):** Receives output from the Trellis Encoder and splits it into multiple parallel paths.
- OFDM MODULATOR (852c):** Each parallel path goes through a **MODULATOR** (4a f1, 4b f2, etc.) and then an **FFT** block (40).
- FDM (40d):** Combines the outputs from the FFT blocks.
- UP CON-VERTER (5a):** Converts the FDM signal to an **RF** signal.
- 1-2 C-CDM 1 MODULATION (4a):** Receives input from the FDM block and the **D1-1** block.

**RECEIVER:**

- DOWN CON-VERTER (24a):** Converts the **RECEIVED SIGNAL** to a baseband signal.
- INPUT CIRCUIT (24):** Receives the baseband signal.
- OFDM DEMODULATOR (852d):** Each parallel path goes through a **FFT** block (40e) and then a **DEMODULATOR** (4a f1, 4b f2, etc.).
- FDM (40b):** Combines the outputs from the demodulators.
- C-CDM DEMODULATION (4b):** Receives input from the FDM block and the **D1-1** block.
- OUTPUT SECTION (758):** Receives output from the C-CDM demodulation and splits it into multiple parallel paths.
- 1st DATA STREAM OUTPUT (758a):** Receives output from the 1st path, passes it through **ECC** and **HIGH GAIN** blocks, and then through a **D1-1** block.
- 2nd DATA STREAM OUTPUT (759b):** Receives output from the 2nd path, passes it through **ECC** and **MAL GAIN** blocks, and then through a **D1-2** block.
- TRELLIS DECODER (759a):** Receives inputs from the **D1-1** and **D1-2** blocks.
- VIDEO DECODER (402a):** Receives output from the Trellis Decoder and splits it into multiple parallel paths.
- 1st VIDEO DECODER (402c):** Receives output from the 1st path.
- 2nd VIDEO DECODER (402b):** Receives output from the 2nd path.
- SUMMER:** Receives inputs from the 1st and 2nd video decoders.
- Outputs:** The summer produces **(LDTV)**, **(EDTV)**, and **(HDTV)** signals.

**FIG. 144**

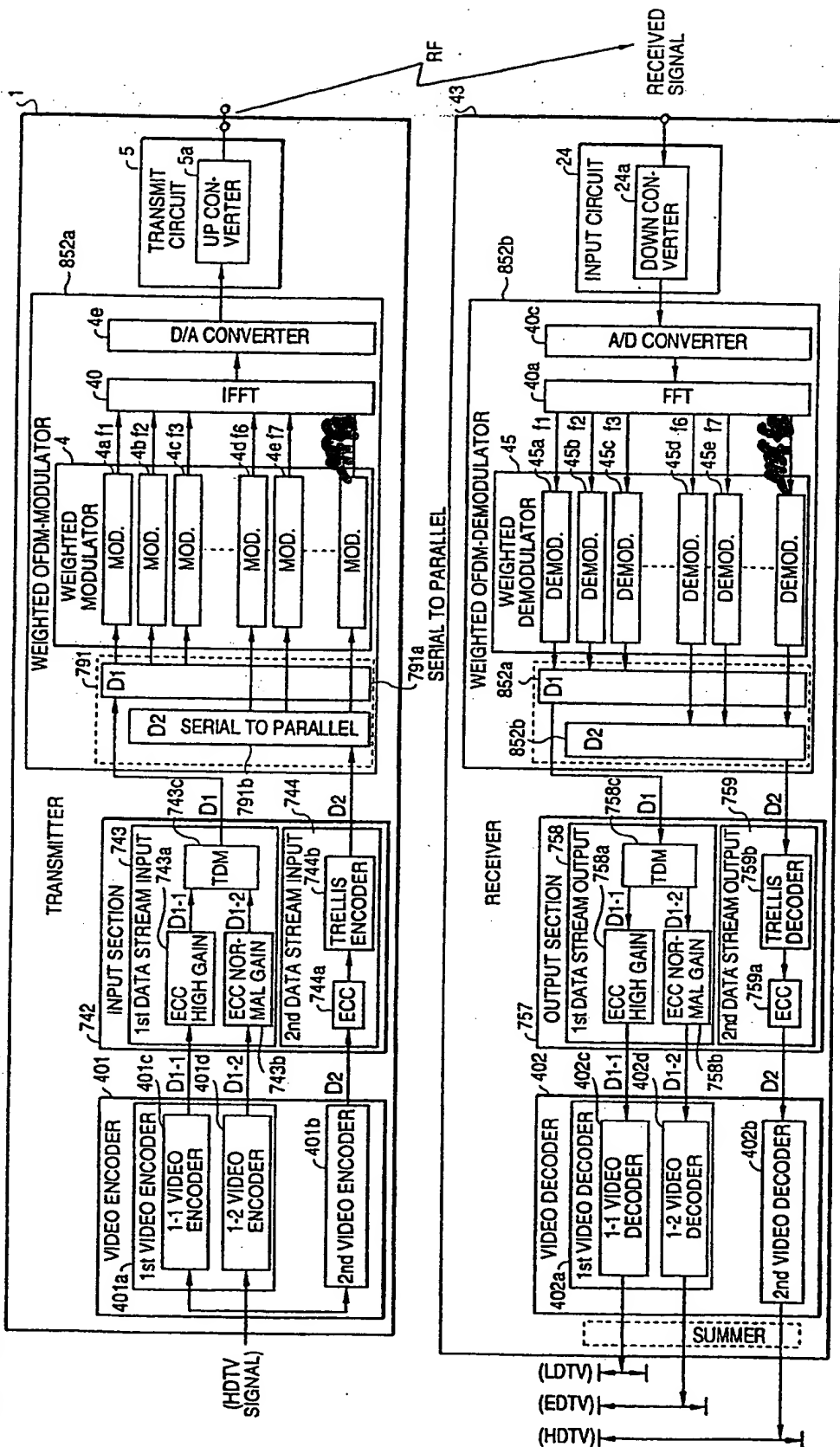


FIG. 169

